Ignition Gate Drive IC

FAD1110-F085

1

SOIC8
CASE 751EB

Description

The FAD1110-F085 is designed to directly drive an ignition IGBT and control the current and spark event of the coil. The coil current is controlled via the input pin. When the differential input is driven high, the output of the FAD1110-F085 is enabled to turn on the IGBT and start charging the coil.

An input spike filter suppresses differential input signals of less then 13 µs in duration. A Max Dwell timer is included in the FAD1110-F085 which will turn off the IGBT if the input stays active for longer than the programmed time. This time interval can be modified through an external capacitor. When the Max Dwell timer is exceeded, the FAD1110-F085 will enter a Hard-Shut-Down mode (HSD) and turn off the IGBT immediately. The FAD1110-F085 will also limit the collector current of the IGBT to $I_{C(lim)}$ during charging. This again is done through the sense resistor in the emitter leg of the Ignition IGBT developing a signal input to the V_{SENSE} pin of the FAD1110-F085.

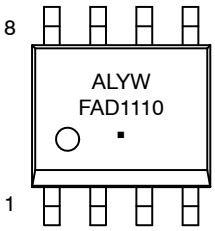
Features

- Differential Input for Ground Shift Disturbances Suppression
- Signal Line Input Buffer
- Input Spike Filter
- Operation from Ignition or Battery Line
- Ground Shift Tolerance – 2 V to 3 V
- Programmable Maximum Dwell Time
- Control IGBT Current Limiting through V_{SENSE} Pin
- Hard Shutdown Following Max Dwell Time Out
- This is a Pb-Free Device

Applications

The FAD1110-F085 is an advanced Ignition IGBT control IC available in a SO8 package or die sales. This full featured Smart Ignition IGBT Driver is particularly advantageous in “switch on coil” applications where size and system performance of the ignition driver are important.

MARKING DIAGRAM



FAD1110	= Specific Device Code
AL	= Assembly Lot Code
Y	= Year
W	= Work Week
▪	= Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Shipping†
FAD1110-F085	−40 °C to 150 °C	8-SOIC	2500 units / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Recommended External Components

TYPICAL EXTERNAL COMPONENTS

Component	Description	Vendor	Parameter	Typ.	Unit
R_{BAT}	Limits transient currents during load dump		R	200 to 300	Ω
C_{BAT}	Battery or Ignition voltage filtering		C	0.47	μF
C_{BAT1}	Battery noise transients		C	10	nF
C_{INC}	Noise immunity		C	10	nF
C_{IND}	Differential mode Noise immunity		C	1	nF
R_{SENSE}	Sense the collector current		R	20	mΩ
R_{INH}	Input Res High		R	1	kΩ
R_{INL}	Input Res Low		R	1	kΩ
R_{IN}	Adjust input impedance		R		Ω

Typical Application

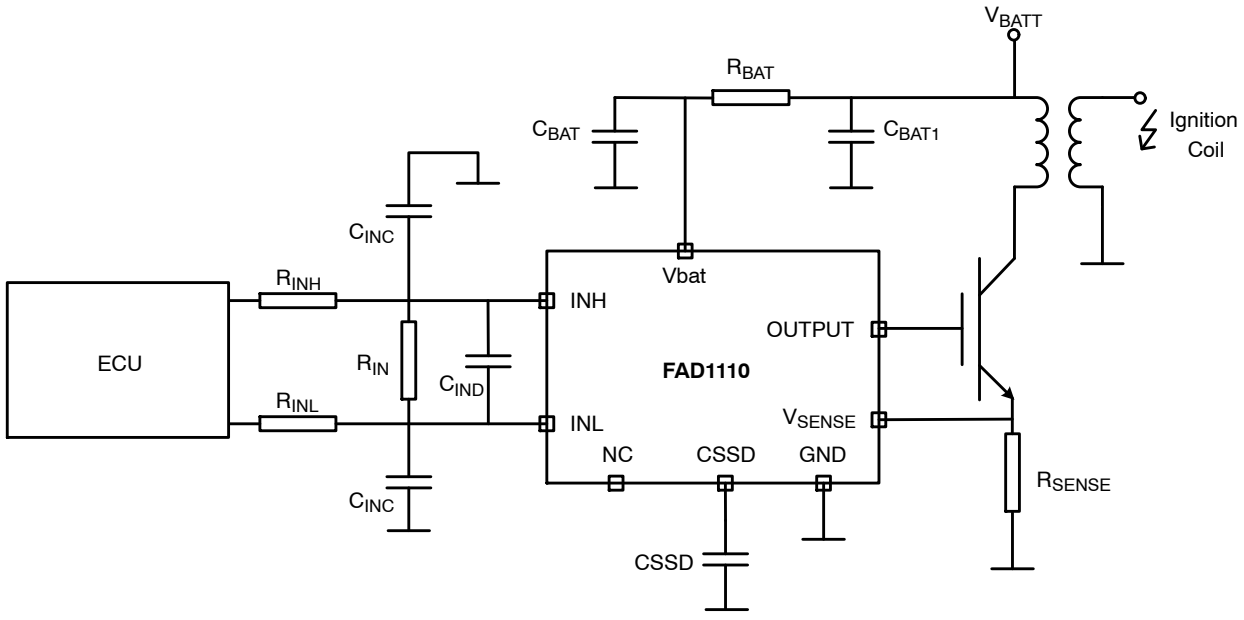


Figure 1. Typical Application

Block Diagram

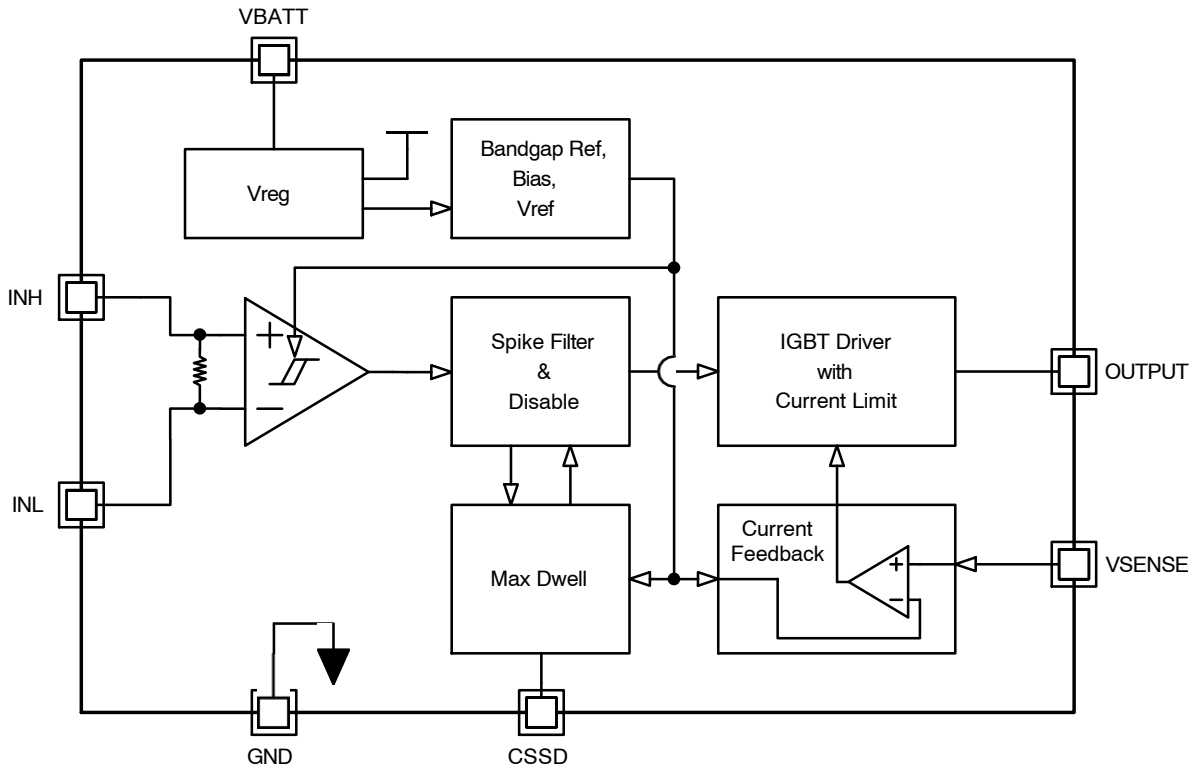


Figure 2. Block Diagram

Package Outline

The FAD1110-F085 is assembled in an 8 lead SOIC Package.

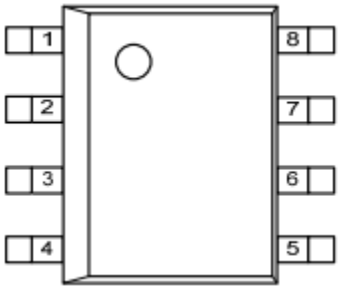


Figure 3. Pin Assignment (Top View)

PIN DESCRIPTION

Name	Type	Description
Pin1	GND	Ground Reference of the Control IC
Pin2	INL	Input ground signal
Pin3	INH	Positive input signal referenced to INL
Pin4	CSSD	Adjust maximum dwell time (to external capacitor)
Pin5	NC	
Pin6	Output	Gate Drive to the IGBT
Pin7	V_{SENSE}	Sense Input used for Ilim function
Pin8	V_{BAT}	Supply voltage

ABSOLUTE MAXIMUM RATINGS (−40 °C to 150 °C unless otherwise stated)

Symbol	Parameter	Min.	Max.	Unit
V_{BAT}	Voltage at V_{BAT} pin (excl. EMC transients)	−0.3	28	V
V_{INH}	Voltage at Input pin High	−5	18	V
V_{INL}	Voltage at Input pin Low	−5	18	V
V_{CSSD}	Voltage at C_{SSD}	−0.3	3.6	V
V_{OUTPUT}	Voltage at Gate Output	−0.3	6.5	V
V_{SENSE}	Voltage on V_{SENSE} pin	0	400	mV
T_J , T_{STG}	Operating and Storage Temperature Range	−40	150	°C
P_{MAX}	Maximum power dissipation (continuous) at T_C = 25 °C		0.625	W
$R_{\theta JC}$	Thermal Resistance − Junction-to-Case (typical)		200	°C/W
V_{ESD} (pin to pin incl. V_{INH} and V_{INL})	Electrostatic Discharge Voltage (Human Body Model) according to MIL STD 883D, method 3015.7 and EOS/ESD Assn. standard S5.1 − 1993		2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS (Reference Load Characteristics) (Note 1)

Symbol	Characteristic	Min.	Typ.	Max.	Units
I_{Ctyp}	Collector (Coil) Operating Current		12		A
L_P	Coil Primary Inductance		1.5		mH
R_P	Coil Primary Resistance (25 °C)		0.4		Ω
R_{LOAD}	Load Resistance (for delay time measurements)		2		Ω

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. **onsemi** does not recommend exceeding them or designing to Absolute Maximum Ratings. (–40 °C to 150 °C unless otherwise stated)

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLY CONDITIONS V_{BAT} = 6 to 28 V ; T_J = –40 °C to 150 °C (unless otherwise specified)						
V_{BAT1}	Operating voltage	Coil switching function	4		28	V
V_{BAT2}	Operating voltage	All functions	6		28	V
I_{BAT}	Supply current	T_J = 150 °C, V_{BAT} = 28 V, Input = 5 V			4	mA
V_{CLAMP}	$V_{BATTERY}$ clamp	I_{BATT} = 10 mA	33		40	V
SENSE PIN CONDITIONS V_{BAT} = 6 to 28 V ; T_J = –40 °C to 150 °C (unless otherwise specified)						
V_{LIMIT}	Sense Voltage at current limit		200	220	240	mV
T_{SPIKE}	Input spike filter	Delay on rising and falling edge of Input		13		µs
T_{D1}	Turn on delay time	(Time from Input = 4.0 V to V_{OUT} = 4.0 V)		17		µs
T_{D2}	Turn off delay time	(Time from Input = 0.5 V to V_{C-GND} = 1.0 V)		17		µs
INPUT CONTROL CONDITIONS V_{BAT} = 6 to 28 V; T_J = –40 °C to + 150 °C (unless otherwise specified)						
V_{INLD}	Differential Input low voltage	INL = GND	1.3	1.7	2.1	V
V_{INHD}	Differential Input high voltage	INL = GND	1.7	2.2	2.7	V
V_{INHys}	Input voltage hysteresis		0.25	0.5	0.75	V
I_{IN}	Input current	V_{BAT} = 0 V, INL = GND		0.10xV_{INH}		mA
I_{IN}	Input current	6 V < V_{BAT} < 20 V, INL = GND		0.10xV_{INH}		mA
V_{CM}	Common mode voltage	Between V_{INH} and V_{INL} reference to GND	–2		3	V
V_{INHGF}	Floating INH voltage	(6 V < V_S < 20 V_{INH} and INL floating) refer to GND @ T = 25 °C		0.5		V
V_{INLGF}	Floating INL voltage	(6 V < V_S < 20 V_{INH} and INL floating) refer to GND @ T = 25 °C		0.5		V
GATE OUTPUT VOLTAGE MAX V_{BAT} = 6 to 28 V; T_J = –40 °C to 150 °C (unless otherwise specified)						
V_{GMAX}	Vgate max	16 KΩ pulldown resistor	4.5	5.4	6	V
V_{GLOW}	Vgate low	(0 mA < I_{GATE} < 0.4 mA @ T = 25 °C)	0.0		0.4	V
DIAGNOSTIC FUNCTIONS AND PROTECTION V_{BAT} = 6 to 28 V ; T_J = –40 °C to 150 °C (unless otherwise specified)						
$CSSD_{MIN}$	Minimum dwell time capacitor			5		nF
TD_{MAX}	Maximum dwell time	(CSSD = 50 nF)	65	100	135	ms
I_{CSSD1}	CSSD Pin current for TDMAX		0.75	1.0	1.25	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

Input and Spike Filter

When the differential input signal voltage between INH and INL pins reaches V_{INHD}, the IGBT will be switched on charging the coil. When this differential input voltage goes below V_{INLD}, the coil current through the IGBT will be turned off. Positive and negative spikes of less than T_{SPIKE} duration at the input line will be filtered out and will not turn on/off the IGBT.

Maximum Dwell Time and Hard-Shutdown (HSD)

When the IGBT is turned on, a delay timer, dependent on the value of the external CSSD capacitor (see Figure 5), is started. If a valid falling edge has not been received after the time T_{DMAX}, the IGBT will be turned off immediately as shown in Figure 4.

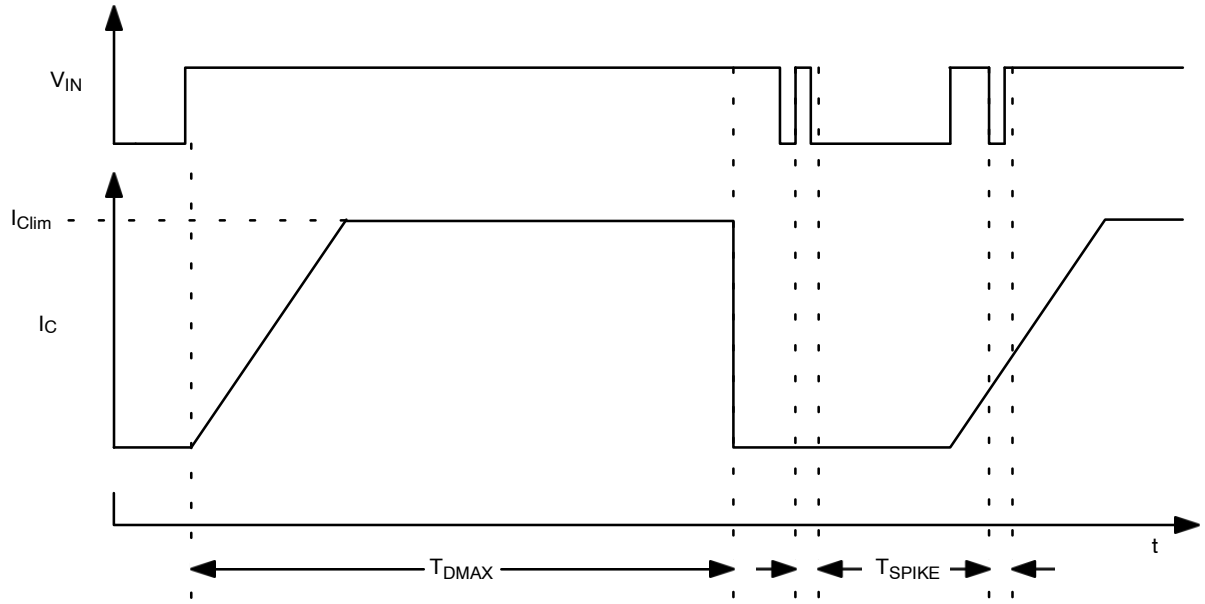


Figure 4. Dwell Time and Hard-Shut-Down

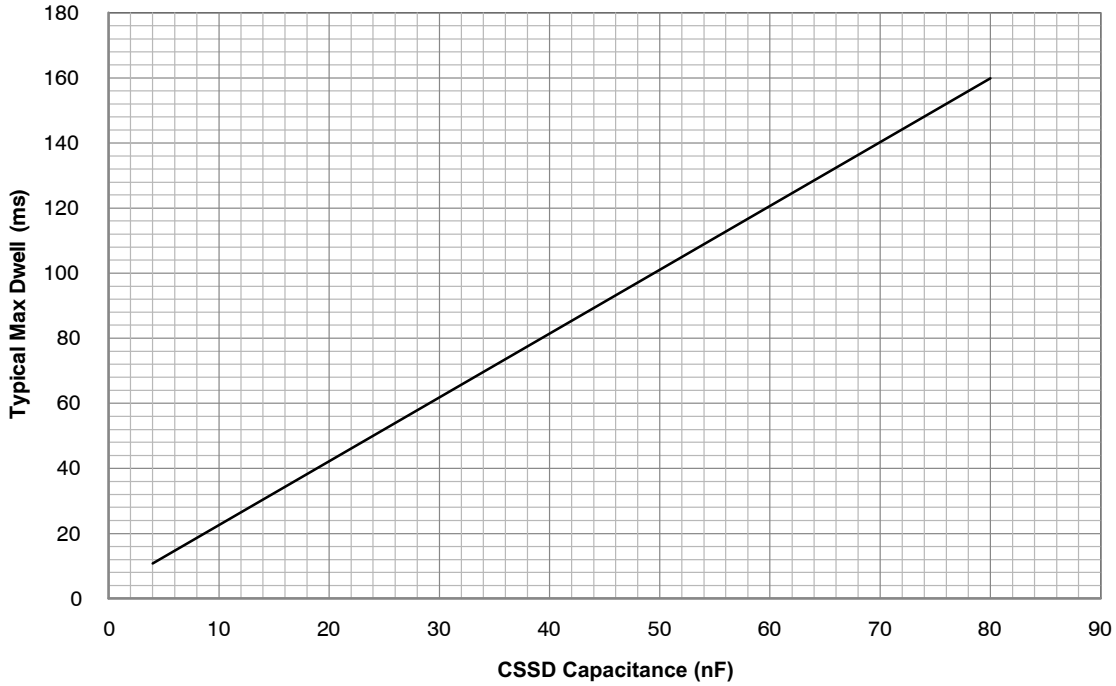


Figure 5. T_{DMAX} as Function of External CSSD Capacitor

REVISION HISTORY

Revision	Description of Changes	Date
1	Figure 1 updated.	3/4/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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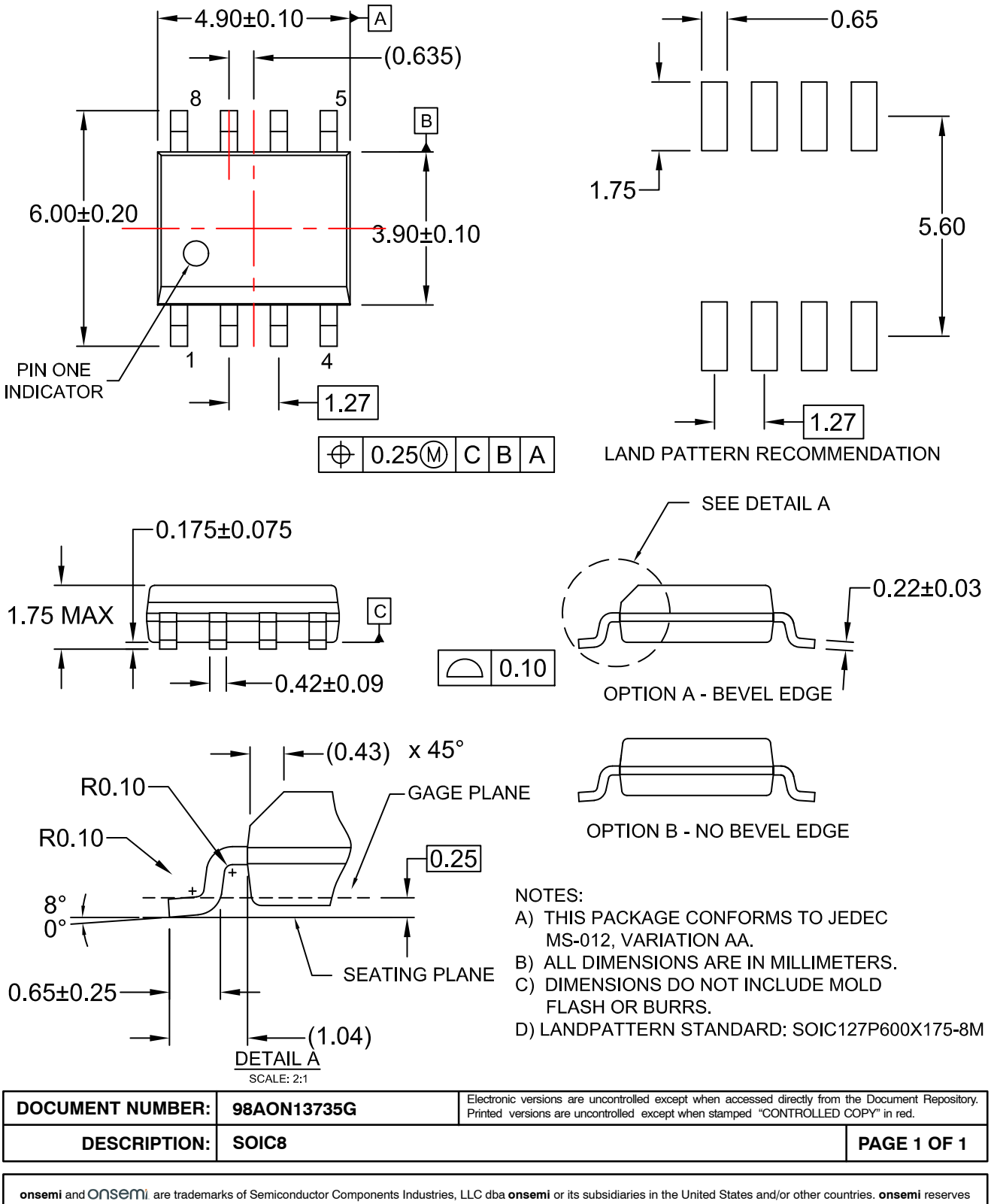
DATE 24 AUG 2017



NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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