



System Solution Guide - Preview

# On Board Charger (OBC)



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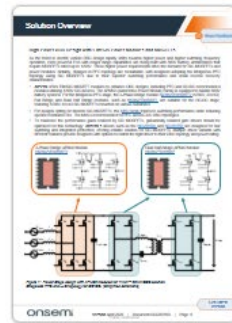
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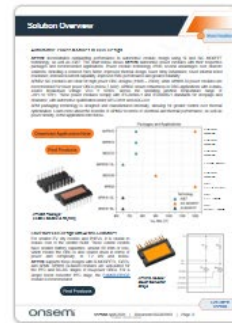
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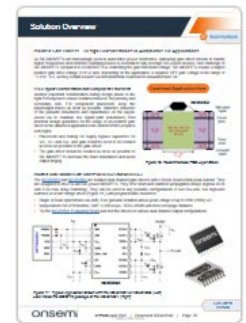
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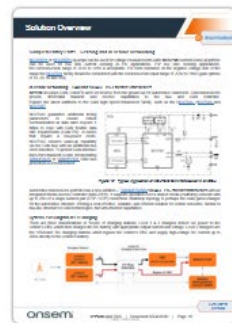
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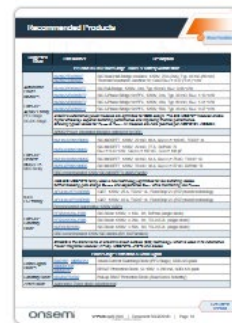
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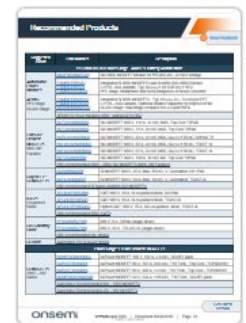
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# Block Diagram - OBC

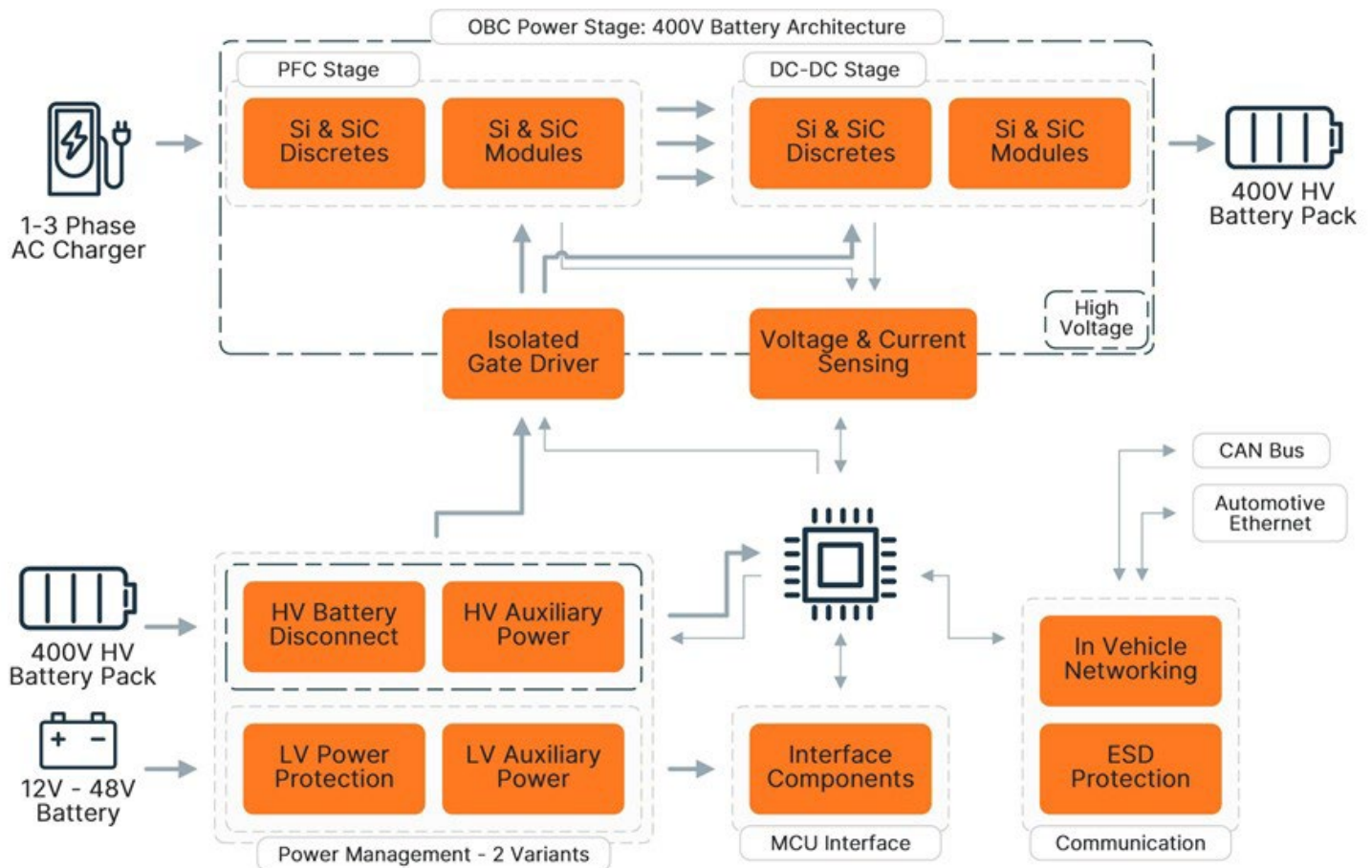
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## Block Diagram – On Board Charger

On Board Charger power stages (PFC and DC-DC) use different power components depending on EV battery pack architecture. Multiple power switching device types are available for all OBC power ratings. Si MOSFETs, modules, or IGBTs are ideal for low-power OBCs, while SiC MOSFETs and modules meet the highest design requirements for high-power OBCs, enhancing thermal performance, efficiency, and power density. The higher switching frequency of SiC devices reduces the size of passive components in the powertrain system, including the DC-link capacitor, inductors, and EMI filter.

The diagram below illustrates a [400V EV battery architecture](#), which requires power switching devices rated up to 650V. Voltage margin is necessary to handle high currents and voltage transients. The interactive block diagram tool also includes a diagram variant for [800V EV battery architecture](#), featuring power discretes and automotive power modules rated up to 1200V.

Isolated gate drivers and voltage/current sensing for signal feedback complete the OBC power stage. The interactive block diagram also includes auxiliary power supplies, LDOs, SmartFETs for power management and protection. CAN and 10BASE-T1S transceivers ensure fast and reliable communication within the automotive network.



Use our Interactive Block Diagrams Tool



Open IBD Tool

## How EliteSiC MOSFETs Improve OBC Performance

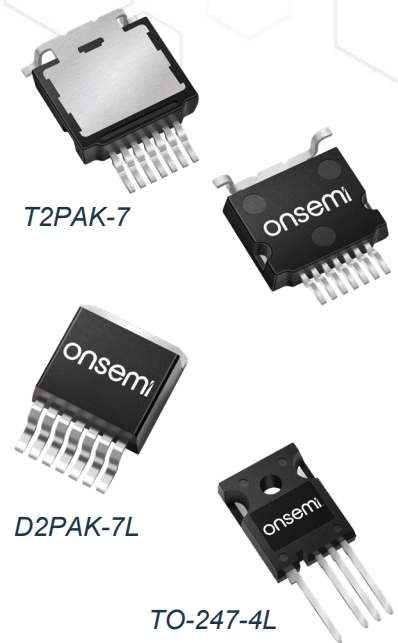
As the trend in electric vehicle OBC design moves rapidly to higher power and higher switching frequency operation, the demand for SiC MOSFETs for this application is also growing. Designers are adopting bridgeless PFC topologies using SiC MOSFETs due to their superior switching performance and small reverse recovery characteristics. The 1200V EliteSiC MOSFETs are extensively utilized in 800V battery architectures. EliteSiC is the brand name of **onsemi's** SiC technology.

### Enhancing AC/DC and DC/DC Switching Performance M3S Family of EliteSiC MOSFETs

**onsemi's** M3S is the latest generation of 1200V and 650V EliteSiC MOSFETs, designed to enhance switching performance while reducing specific resistance  $R_{SP}$ . The M3S series strikes an excellent balance between conduction and switching losses, making it ideal for hard-switching applications like PFC.

Additionally, the low  $R_{DS(ON)}$  values of M3S MOSFETs position them as strong contenders for soft-switching applications (such as LLC, CLLC, Phase Shifted Full Bridge), where switching losses are significantly reduced by virtue of the circuit topology, so that conduction losses become the dominant loss component. The mature planar design ensures no drift in  $R_{DS(ON)}$ ,  $V_{GS(TH)}$  or body diode voltage drop over MOSFET lifetime, and reliable operation with negative gate drive voltages.

Explore in-depth comparison of M1 and M3S 1200V SiC families in the attached AND90204 Application Note. In the exploration focusing on 1200V MOSFETs, the M3S family requires less total gate charge  $Q_{G(TOT)}$  than the 1<sup>st</sup> generation M1, which significantly reduces the amount of sinking and sourcing current from gate drivers, as shown in Figure 2. The M3S further reduces Figure of Merit (FOM) factor in  $R_{DS(ON)} * Q_{G(TOT)}$  by 44% compared to its older M1 counterpart.



[Download Application Note](#)

Figure 3. shows the improved switching performance of M3S under given conditions, with 40% lower  $E_{OFF}$ , 20–30% lower  $E_{ON}$ , and 34% lower total switching loss than M1. In high switching frequency applications, this will offset any potential disadvantage of higher  $R_{DS(ON)}$ .

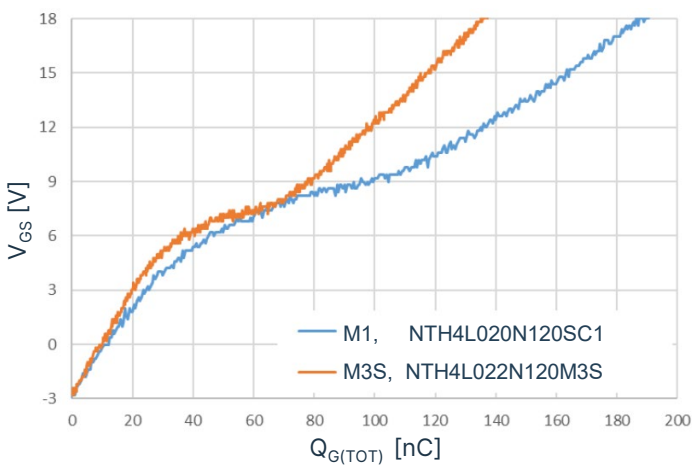


Figure 2: Total Gate Charge  $Q_{G(TOT)}$  [nC]  
@  $V_{DS} = 800V / 40A$ , driven by constant 10mA

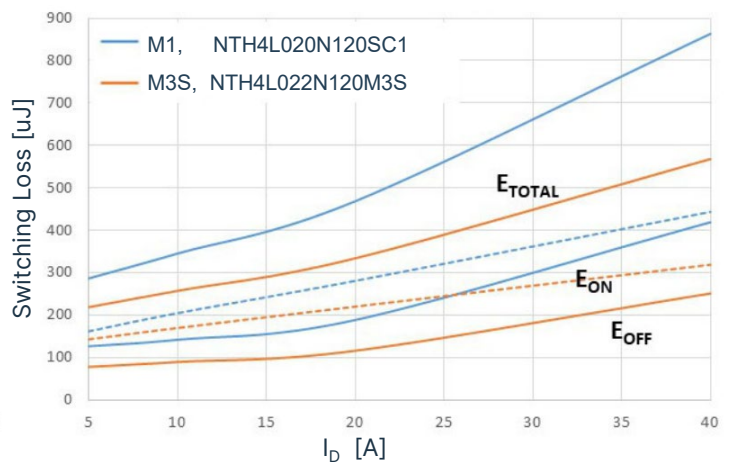


Figure 3: Switching Losses by drain current  $I_D$  [A]  
@  $V_{DS} = 800V$ ,  $V_{GS} = -3V / 18V$ ,  $R_G = 4.7 m\Omega$

## Unlock Higher Power Density and Thermal Performance with Top-Side Cooling

To meet the ever increasing demands of OBC applications, such as higher power density, lower losses, and rock-solid reliability, **onsemi** has introduced new EliteSiC MOSFETs in top-side cooled T2PAK package. Unlike bottom-side cooling packages such as D2PAK and TOLL, which require power extraction through the printed circuit board (PCB), the T2PAK utilizes top-side cooling. This design ensures direct thermal contact with the heatsink, significantly improving thermal performance.

With its top-side cooling and leadless design, T2PAK minimizes stray inductance by eliminating long leads and enabling tighter current loops than D2PAK or TO-247 packages. This results in improved switching behavior, reduced voltage overshoot and better EMC performance. This advancement allows for higher power density, addressing the needs of high-performance automotive applications and thermally constrained designs.

Find guidance for hardware engineers working on OBC, HV DC/DC systems and learn about mounting T2PAK package, soldering considerations and leveraging its thermal properties in the [T2PAK Design application note](#).

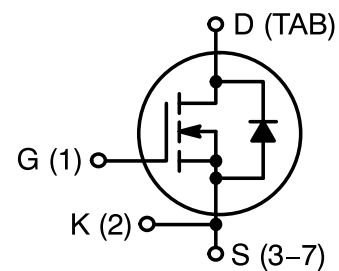
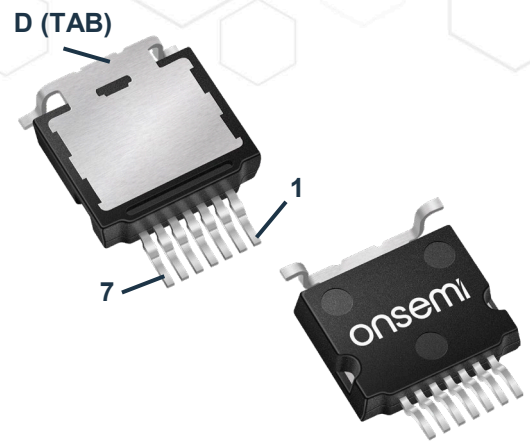


Table 2 : Key Specifications of EliteSiC MOSFETs in T2PAK

Product PN	Main Features
<a href="#">NVT2012N065M3S</a>	$V_{DSS}$ 650 V, 112 A, 12 m $\Omega$ , M3S tech.
<a href="#">NVT2016N065M3S</a>	$V_{DSS}$ 650 V, 72 A, 16 m $\Omega$ , M3S tech.
<a href="#">NVT2023N065M3S</a>	$V_{DSS}$ 650 V, 72 A, 23 m $\Omega$ , M3S tech.
<a href="#">NVT2016N090M2</a>	$V_{DSS}$ 900 V, 148 A, 16 m $\Omega$ , M2 tech.

### Optimizing Thermal and Electrical Design with T2PAK

Top-side thermal path provides an efficient and controlled heat dissipation mechanism, especially in applications where PCB thermal capacity is limited or where forced air cooling is available on the component side. Ability to offload heat directly to a heatsink bypasses the thermal limitations of the PCB. This makes T2PAK particularly well-suited for automotive environments that require enhanced thermal headroom.

Achieving peak system performance requires a robust thermal interface between the exposed drain pad and the heatsink. Beyond the junction-to-case resistance ( $R_{\theta JC}$ ), overall thermal behavior also strongly depends on proper thermal stack-up and the selection of high-conductivity thermal interface material (TIM). Accurate TIM application ensures consistent thermal performance and long term reliability. Learn more in the [T2PAK Design application note](#).

Top-cooled packages also provide a distinct opportunity to reduce parasitic inductance within commutation loops compared to bottom-cooled packages. This design enables more flexible electrical routing on the PCB, tighter and better optimized commutation current loop, directly contributing to reduced switching losses and higher overall system performance. Figure 4. shows a complete commutation loop in a half-bridge.

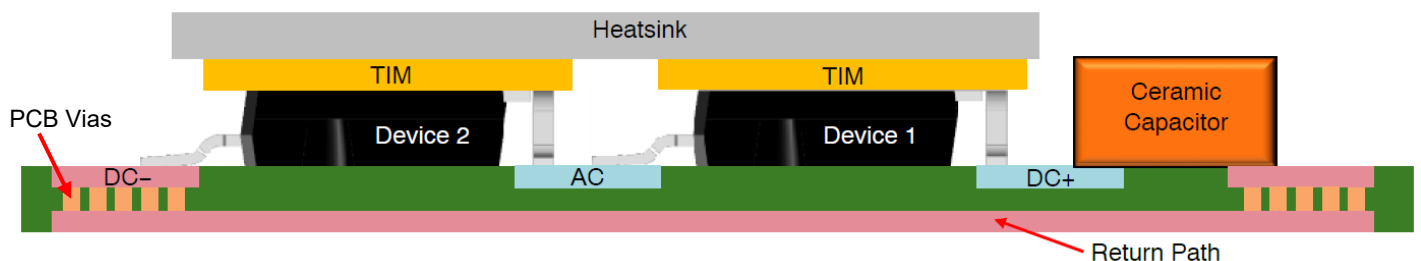


Figure 4: Half-bridge configuration with T2PAK MOSFETs. Current return path can be routed through the bottom layer of the PCB - illustration of a compact commutation loop geometry.

## Isolated Gate Drivers – Design Considerations in Automotive HV Applications

As SiC MOSFETs are increasingly used in automotive power electronics, optimizing gate driver circuits to handle higher frequencies and minimize switching losses is essential to fully leverage SiC power devices. One challenge of SiC MOSFETs compared to Si MOSFETs is controlling the gate threshold voltage. SiC MOSFETs require a higher positive gate drive voltage (+20 V) and, depending on the application, a negative OFF gate voltage in the range of -2 V to -6 V, as they exhibit a lower  $V_{GS}$  threshold that could lead to unwanted turn-on.

### PCB Layout Consideration and Component Placement

Another important consideration during design phase is the right PCB layout to ensure isolation between the primary and secondary side. For component placement, keep the input/output traces as short as possible. Minimize influence of the parasitic inductance and capacitance on the layout. (avoid via to maintain low signal-path inductance) Find practical design guidelines on the usage of an isolated gate driver in the attached application note AND90180/D (requires web login).

- Placement and routing for supply bypass capacitors for  $V_{DD}$ ,  $V_{CC}$  and  $V_{EE}$ , and gate resistors need to be located as close as possible to the gate driver.
- The gate driver should be located as close as possible to SiC MOSFET to decrease the trace inductance and avoid output ringing.

Download Application Note

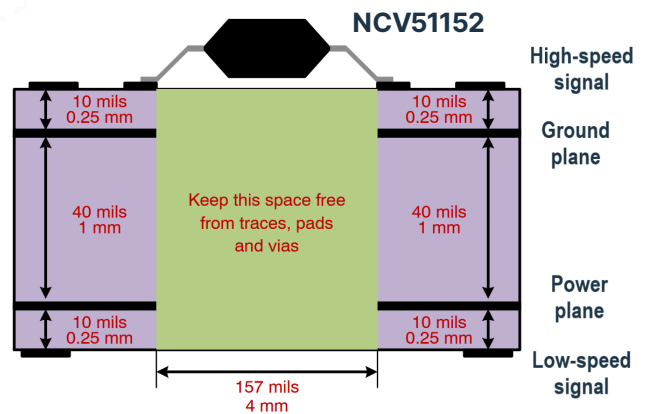


Figure 10. Recommended PCB Layer Stack.

### Isolated Dual Channel Gate Drivers NCV51561 and NCV51563

The [NCV51561](#) and [NCV51563](#) are isolated dual channel gate drivers with 4.5A/9A Source/Sink peak current. They are designed to drive Si and SiC power MOSFETs. They offer short and matched propagation delays (typical 36 ns with 5 ns max delay matching). They can be used in any possible configurations of two low-side, two high-side switches or a half-bridge driver (Figure 11.) with programmable dead time.

- Single or Dual Input Modes via ANB, 5 kV galvanic isolation allows peak voltage of up to 1500 (1850)  $V_{DC}$
- Independent UVLO Protection,  $CMTI \geq 200 \text{ kV}/\mu\text{s}$ , SOIC-16WB with 8mm creepage distance.
- Try the [NCV51561 Evaluation Board](#) and test the drivers in various dual channel output configurations.

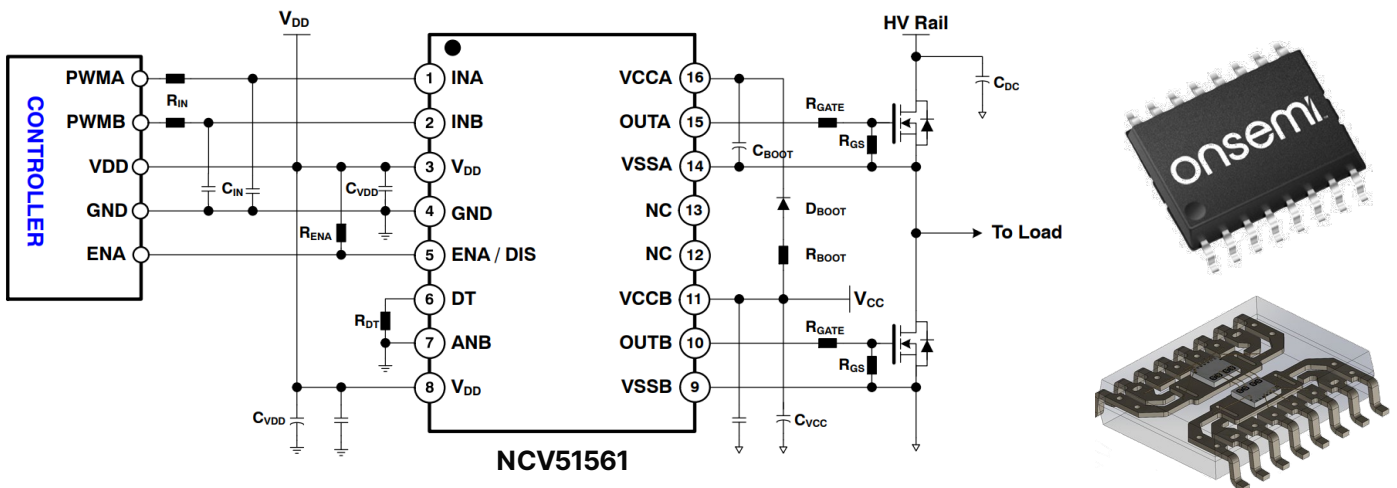


Figure 11: Typical Application Circuit with the NCV51561 or NCV51563. (Left) Look inside the SOIC-16 package of the NCV51561. (Right)

# Frequently Asked Questions (FAQ)

## What is the scope of the On Board Charger (OBC) System Solution Guide from onsemi?

**1** The On Board Charger System Solution Guide (SSG) provides a comprehensive overview of OBC architectures used in BEV and PHEV platforms. It covers market trends, system block diagrams for 400 V and 800 V battery architectures, power stage topologies. Furthermore, find detailed guidance on **onsemi's** power modules, discrete MOSFETs, isolated gate drivers, sensing and networking. The guide supports scalable, automotive-qualified OBC designs from 7 kW up to 22 kW and beyond.

## How does onsemi support high-power OBC designs using APM32 Automotive Power Modules?

**2** **onsemi's** APM32 Automotive Power Modules enable compact, high-power OBC designs in the 11 kW to 22 kW range, optimized for 400 V to 800 V EV battery systems. These SiC based modules integrate 1200 V EliteSiC MOSFET dies with low stray inductance and optimized thermal paths, improving efficiency, power density and EMC performance. APM32 modules are constructed to simplify PFC and DC-DC stages while meeting stringent automotive qualification and reliability requirements.

## Why are isolated gate drivers critical in modern OBC designs, especially with SiC MOSFETs?

**3** Isolated gate drivers are essential in OBC designs to safely control high-voltage SiC MOSFETs while protecting low-voltage control electronics. **onsemi's** isolated gate drivers support high CMTI, reinforced isolation and negative gate bias control. This enables mitigating parasitic turn-on caused by fast  $dv/dt$  and Miller capacitance. These features improve switching robustness, efficiency, functional safety and critical fault prevention in high-power automotive OBC modules.

## What benefits do onsemi's discrete T2PAK top-side cooled MOSFETs bring to OBC applications?

**4** T2PAK top-side cooled MOSFETs are designed to unlock higher power density and improve thermal performance in OBC and HV DC-DC designs. By transferring heat directly from the MOSFET drain to the heatsink, T2PAK avoids PCB thermal limitations, reduces junction temperature and enables tighter commutation loops via optimized PCB routing. This results in improved efficiency, reduced EMI and better thermally optimized OBC power stage.

## How do onsemi EliteSiC M3S MOSFETs improve OBC performance compared to earlier M1 and M2 generations?

**5** EliteSiC M3S MOSFETs are optimized for high-speed switching stages in OBC PFC and DC-DC converters. Compared to M1 and M2 generations, M3S devices feature significantly reduced total gate charge ( $Q_G$ ), lower switching energy ( $E_{ON}/E_{OFF}$ ) and improved  $R_{DS(ON)} \times Q_G$  figure-of-merit. The M3S design focuses on minimizing switching losses at high  $dv/dt$  and  $di/dt$ , enabling higher switching frequencies, smaller magnetics, reduced EMI filtering and increased power density in 11–22 kW OBC architectures.

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